What is claimed is:

1. A structure comprising:

a shaped clock signal generator means said shaped clock generator being synchronous or asynchronous with the data bit rate received by a data signal receive input port; and

a data signal receiver port and processor for providing control signal generation means for selecting the said shaped clock signal for further transmission and/or modulation.

2. A structure comprising:

a splitter receiving an input signal and splitting said input signal into two or more signal streams;

a clock generator for receiving one of the said signal streams and generating a clock signal;

one or more shaped clock generator means for receiving said clock signal and for generation of one or more shaped clock signals;

a set of input ports for receiving shaped clock signals;

a selector switch for selecting one of the shaped clock signals, said selector switch having an input interface port connected to the data-based selection control signals and another set of input ports connected to the shaped clock signals; and

an output interface port coupled to said selector switch output.

3. An architecture comprising:

a data interface input for receiving input data and for providing an input data-based clock selector data signal;

a set of input ports for receiving a set of shaped clock signals and of not-shaped clock signals;

a set of one or more clock generators which differ in one or more clock parameters from each other;

a selector switch for selecting one of the processed clock signals; and

a data interface output port for receiving said selected signal and providing it to the transmitter circuitry.

4. A structure comprising:

a clock generator which provides clock signals to two or more clock transition time shifting and clock shaping signal generators;

a data input port and connection to a data interface input encoder for the generation of clock selector data signal by said data input interface encoder;

a switch to choose, based on said clock selector data signal, one of the clock transition time-shifted shaped clock signals and connect the selected signal to the data interface output unit; and

a data interface output unit for connecting the selected signal to the transmission medium or further signal processing.

5. A transmit signal processor structure comprising:

a first clock signal generator having a first set of clock shaping parameters;

a second clock signal generator having a second set of clock shaping parameters, said second set of clock shaping parameters having at least one parameter different from that of the first set of clock signal shaping parameters;

a data input receive circuitry and processor for selection of one of the said first or second clock shaped signals;

a switch for switching between the first set and second set of shaped clock parameters; and

an output interface port to provide the selected signal to the transmission medium.

6. A spectral saving data and clock signal processing system comprising:

data signal and clock signal processing means to provide a clock modulated signal having changeable distances between the rising edges and falling edges of the modulated clock signals; and

control means having its input connected to the data signal source and its output connected to edge distance switch selection means; and

digital interface output means to connect the clock modulated signal to the interface of the subsequent signal processor.

7. A clock signal modulator comprising:

a data input interface means to provide data signals to an asynchronous pure clock source;

an asynchronous pure clock generator means to provide a pure clock signal; and

a selector switch means which is controlled by the data interface means to provide a shorter distance between the falling edge and rising edge of the clock modulated signal for a zero state data signal and a longer distance between the falling edge and rising edge of the clock modulated signal for a one-state data signal.

8. A clock converter system comprised of:

an input data interface means for controlling the selection process of the shaped clock signal which is provided to the interface output unit means;

a clock signal shaping means to provide smoothed continuous clock signals to the clock signal selection means having one or more different clock signal parameters; and

an output signal processing means to accept the smoothed different clock signal parameter processed clock converted signals.

9. A clock modulated signaling system comprising:

an input data interface means to provide control signal generation and selection means of shaped clock signals;

an interface means to provide signal processing means for modulating the clock modulated baseband signal by means of a cross-correlated quadrature modulator system;

an output amplifier means to connect the cross-correlated quadrature modulated signal to the transmission medium;

demodulation means to demodulate the received quadrature modulated signal; and

signal processor means to decode and regenerate the clock modulated signal.

10. An architecture comprising:

a data interface input for receiving input data and for providing an input data-based clock selector data signal;

a set of input ports for receiving a set of shaped clock signals and of not-shaped clock signals;

a set of one or more clock generators which differ from each other in one or more clock parameters;

a selector switch for selecting one of the processed clock signals; and

a data interface output port for receiving said selected signal and providing it to the transmitter circuitry.

11. A method comprising steps:

receiving a data signal;

generating a shaped clock signal in response to said received data signal;

generating a control signal for selecting said generated shaped clock signal; and

processing said selected shaped clock signal for transmission or modulation.

12. The method in Claim 11, wherein said shaped clock signal is generated synchronously with a data bit rate of said received data signal.

13. The method in Claim 11, wherein said shaped clock signal is generated asynchronously with a data bit rate of said received data signal.

14. A method of signaling using clock modulated signals, said method comprising:

selecting at least one shaped clock signal;

cross-correlating and quadrature modulating said selected at least one shaped clock signal;

amplifying said cross-correlated quadrature modulated signal;

transmitting said amplified cross-correlated quadrature modulated signal;

receiving said transmitted amplified cross-correlated quadrature modulated signal;

demodulating said received signal; and

decoding said received demodulated signal and regenerating said clock signal.